FPGA Power Estimation Simulator for Dynamic Input Data

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***Abstract* — As the availability of field-programmable gate arrays (FPGAs) increases, the importance of their power management has become crucial. For an efficient power management scheme, an accurate power estimation is required. The power consumption of FPGAs differs depending on the input, and previous power estimation methods have limitations which make it difficult to predict the input patterns which affect the power consumption of FPGA. Therefore, we propose a simulator which is able to estimate the power in consideration of input data. It estimates the power consumption more accurately at a minute level. From the result of experiment, we identify that there is a great gap on power estimation between previous methods and the proposed one.**

Keywords—field-programmable gate array(FPGA); power; estimation; simulator;

I. INTRODUCTION

Field-programmable gate arrays (FPGAs) are reconfigurable logic and are available to use in programming of various applications. However, they usually consume more power compared to application specific integrated circuits (ASICs) since FPGAs consist of many logic blocks, wires, as well as switch boxes which are required to make them reconfigurable [1]. As they are also used in power hungry area such as internet of things (IoT), smartphones and hardware accelerators, the importance of managing the power of FPGA is increasing and thus more accurate power estimation schemes are required.

There exist a few simulation-based and probabilistic-based power estimation methods. Simulation-based ones provide higher accuracy but as they consume more time, i.e. in a day level, as the size of the application programmed in FPGAs increases, the cost of power estimation is quickly becoming a great burden. Probabilistic-based ones predict the activity of each component consisting an FPGA and then calculates its dynamic and static power. The studies are dominated by the ones that enhance the accuracy of power models and probabilistic activity on each component [2]. However, there exist critical issues in these methods. First of all, it is difficult to predict the pattern of input data as applications mapped in FPGAs become complicated are spread in various fields. That is, the power estimation based on the activity prediction of a FPGA component has become less accurate. Secondly, the power consumption of each component differs depending on the input data. For instance, the variability of power consumption can be as high as 69% with 4 input LUT depending on the input data [3]. Finally, it is impossible to estimate the peak power because the previous power estimations only target to measure the average power. The estimation of the peak power is essential as recent FPGAs are integrated in other power-critical systems.

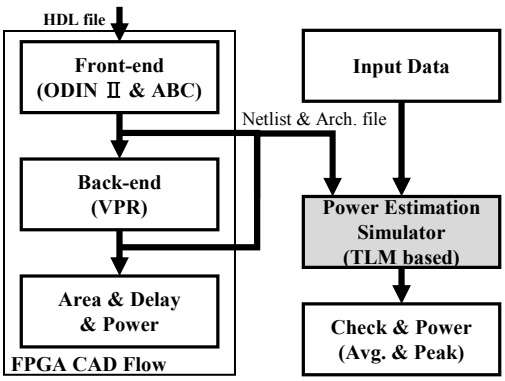

Fig. 1. Proposed Power Estimation flow

In this paper, we design a power estimation simulator based on transaction-level modeling (TLM). It constructs the circuit of target applications using the information provided by FPGA computer-aided-design (CAD) tools and calculates the dynamic and static power every clock through the comparison of the current data and previous data. As a result, it estimates average and peak power in a minute level.

II. POWER ESTIMATION SIMULATOR

A. Power Estimation Methodolgy

A FPGA CAD consists of front and back-end as shown fig. 1. We use ODIN Ⅱ[4], ABC[5], VPR[6] which are popular academic FPGA CAD tools. Although conventional FPGA CAD tools support power estimation, they do not consider the input data. We design a simulator that enables an accurate power estimation considering power variation by input data in a minute level. The simulator, which utilizes the information from CAD tools and FPGA architecture, constructs connections between components in FPGA. Then, it calculates

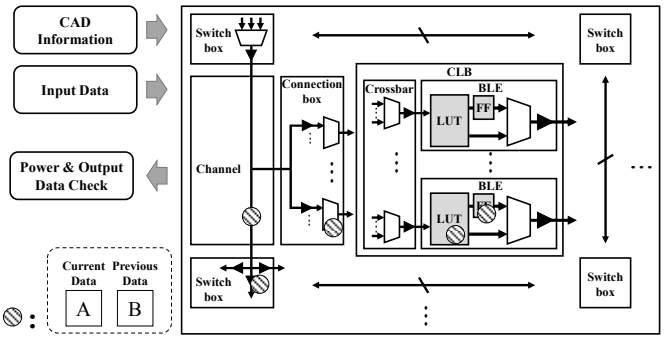

Fig. 2.Proposed Power Estimation constructer

the dynamic and static power of each component according to the input data in order to calculate the average and peak power of the overall system.

As shown fig. 2, the components of FPGA are composed of switch boxes, channels, connection boxes and configurable logic blocks (CLBs) which consist of look-up tables (LUTs), flip-flops and a crossbar logic. These components except the LUTs and the flip-flops are composed of MUXs, buffers and wires. In order to estimate these power components, our simulator stores the current data and the previous data. The power model of each components is provided by VPR CAD tool. The power of each component is divided into dynamic and static power, they are represented by $P_{dynamic}= 1/2CV^2f$ and $P_{static}=VI$, respectively. And the capacitance of each component is determined by FPGA architecture. The power of LUTs and flip-flops are determined according to the in/out data combinations. As for the wires and buffers, the dynamic power consumption occurs upon data toggle (e.g. $0 \rightarrow 1$, $1 \rightarrow 0$). For MUXs, the dynamic power is calculated when data toggle of in/out pin occurs and static power is calculated for unselected pins. Finally, total power can be measured by combining these calculated dynamic and static power. This power modeling method yields a simulator which can measure the average and the peak power consumption of each application and the accuracy would be similar to the real FPGA environment.

To validate our simulator, we compare the output data of proposed simulator with the output data from ModelSim simulation, since the proposed simulator estimates the power depending on changes of input data, the correct functionality is crucial for an accurate power estimation.

III. EXPERIMENT

We identify the applicability of the proposed power estimation simulator by comparing the result of VPR simulation in various applications. Table.1 shows the result of VPR and the proposed simulator using ten thousand input data set. We identify that the maximum difference value between power consumption of VPR and that of dynamic power estimation simulator is 13.13 times. In case of VPR, it estimate the power regardless of input data since it is calculated using toggle probability of each component. However, our proposed simulator has different estimation results depending on input data which enables the peak power estimation.

TABLE I. RESULT OF POWER ESTIMATION

Application	Power (uW)		
	VPR	*Proposed Simulator*	
		Avg.	*Peak.*
Dag3_mod	***1798***	***889.53***	***1261.41***
4_bit_shift_register	***1061***	***383.26***	***638.08***
Logic_w_Dff2	***708.4***	***80.80***	***122.84***
If_common	***1167***	***622.26***	***1074.95***
Stmt_all_mod	***2306***	***718.05***	***956.66***
Stmt_compare_padding	***935.1***	***351.94***	***604.06***

IV. CONCLUSION

In this paper we proposed a simulator which is able to estimate power which depend on input data of applications. Also, through the comparison of the power estimation result of the simulator to the result of VPR, we identify that there were large differences in power estimation. As a future work, we shall apply a high-accuracy power modeling of components to the simulator for a higher accurate power estimation.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (2016R1A2B4011799) and by SK-Hynix Semiconductor Inc.

REFERENCES

[1] Kuon, Ian, Russell Tessier, and Jonathan Rose, "FPGA architecture: Survey and challenges," Foundations and Trends in Electronic Design Automation 2.2, 2008, pp. 135-253.

[2] Tang et al., "FPGA-SPICE: A simulation-based power estimation framework for FPGAs," In: Computer Design (ICCD), 2015 33rd IEEE International Conference on. IEEE, 2015, pp. 696-703.

[3] F. Li et al., "Power Modeling and Characteristics of Field Programmable Gate Arrays," IEEE TCAD, Vol. 24, No. 11, 2005, pp. 1712-1724.

[4] Jamieson, Peter, et al. "Odin II-an open-source verilog HDL synthesis tool for CAD research," FCCM, 2010 18th IEEE Annual International Symposium on. IEEE, 2010. pp. 149-156.

[5] Brayton, Robert, and Alan Mishchenko, "ABC: An academic industrial-strength verification tool," Computer Aided Verification. Springer Berlin Heidelberg, 2010. pp. 24-40.

[6] Betz, Vaughn, and Jonathan Rose. "VPR: A new packing, placement and routing tool for FPGA research," Field-Programmable Logic and Applications. Springer Berlin Heidelberg, 1997, pp.213-22.